AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A process of manufacturing a semiconductor device, the process comprising:

forming elements on a wafer, and thereafter forming an interlayer insulating film on the wafer over at least the elements;

flattening the interlayer insulating film formed by chemical mechanical polishing, [[and]]

wherein a stopper layer is formed only at an edge region of the device so that no layer portion deposited along with the stopper layer remains on the device during the chemical mechanical polishing of the interlayer insulating film at any location other than as part of the stopper layer at the edge region of the device, the stopper layer preventing ~~where otherwise~~ the interlayer insulating film from being ~~would be~~ excessively polished ~~through~~ by the chemical mechanical polishing at the edge region of the device compared to a remainder of the interlayer insulating film,

wherein the stopper layer is formed before or after forming the interlayer insulating film.

2. (Previously presented) A process according to claim 1, wherein the stopper layer has a thickness greater than a thickness of the interlayer insulating film to be obtained in the final product.

3. (Original) A process according to claim 1 further comprising the step of photolithography for forming a connection hole in the interlayer insulating film, wherein the stopper layer has a width greater than that of a resist layer to be removed from a wafer periphery portion in the photolithography step.

4. (Previously presented) A process according to claim 1, wherein the stopper layer comprises silicon nitride.

5. (Previously presented) A process according to claim 1, wherein the interlayer insulating film comprises silicon oxide.

6. (Original) A process according to claim 3, wherein the width of the resist layer to be removed from the wafer periphery portion is 3-4 mm.

7. (Original) A process according to claim 1, wherein the stopper layer is removed after the chemical mechanical polishing.

8. (Previously presented) A process according to claim 2, wherein the stopper layer has a thickness greater than the thickness of the interlayer insulating film in the final product by 50-700 Å.

9. (Currently amended) A method of making a semiconductor device, the method comprising:

forming elements to be at least partially supported by a substrate,

forming a stopper layer so that the stopper layer is located at an edge portion of the device but not at any central portion of the device located proximate a center of the device,

forming an interlayer insulating film over at least the elements and the stopper layer; [[and]]

chemical mechanical polishing the interlayer insulating film so as to remove the interlayer insulating film over the stopper layer, wherein a polishing rate of the interlayer insulating film is greater than a polishing rate of the stopper layer,

wherein no layer portion deposited along with the stopper layer remains on the device during the chemical mechanical polishing of the interlayer insulating film at any location other than as part of the stopper layer at the edge portion of the device, and

wherein the stopper layer prevents ~~so that~~ the interlayer insulating film from being ~~is not~~ excessively polished at the edge portion of the device compared to a remainder of the interlayer insulating film.

10. (Currently amended) A method of making a semiconductor device, the method comprising:

forming elements on a substrate,

forming an interlayer insulating film over at least the elements;

forming a stopper layer over only an edge portion of the interlayer insulating film so that the stopper layer is located at an edge portion of the device but not at any central portion of the device proximate a center of the device;

chemical mechanical polishing the interlayer insulating film and the stopper layer, wherein a polishing rate of the interlayer insulating film is greater than a polishing rate of the stopper layer, so that the interlayer insulating film is prevented from being ~~not~~ excessively polished at the edge portion of the device compared to a remainder of the interlayer insulating film not located at the edge portion of the device; and

after the chemical mechanical polishing, removing the stopper layer from the edge portion of the interlayer insulating film so as to expose a portion of the interlayer insulating film that had previously been under the stopper layer.

11. (New) The process of claim 1, wherein the stopper layer is formed before the interlayer insulating film.

12. (New) The process of claim 1, wherein the stopper layer is formed after and over the interlayer insulating film so as to contact an upper surface of the interlayer insulating film.

13. (New) The process of claim 1, wherein the edge region of the device is an edge region of the wafer.

14. (New) The process of claim 10, wherein the edge region of the device is an edge region of a wafer.